14.3 A Telecom Baseband Circuit based on an Asynchronous Network-on-Chip

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The emerging 4G wireless telecommunication technology poses two inevitable constraints for the chipset design: a high level of integration and algorithm complexity. But even though nanometric CMOS technologies make it possible to integrate the required hardware resources into a single chip, enormous difficulties arise for the on-chip interconnections and the communications between sub-blocks more generally. To address these issues, this paper presents a complete System-on-Chip (SoC) framework based on an asynchronous Network-on-Chip (NoC). The concept is proven in a chip named FAUST (Flexible Architecture of Unified System for Telecom) which supports complex Multi-Carrier OFDM-based telecom applications.

Conventional interconnect techniques derived from bus architectures fail to fulfill the demands of communication services in complex SoCs. These solutions, such as hierarchical bus or crossbars, are synchronous and centralized and face a severe issue: the timing closure of long wires is problematic, and probably not attainable, with the variability present in next generation nanotechnologies. A NoC is intrinsically distributed and satisfies the two basic requirements of SoC intercommunications: high bandwidth and low latency [1]. Furthermore, an NoC provides an efficient decorrelation between communication and computing aspects, which facilitates IP integration. These NoC characteristics are combined here with a Globally Asynchronous Locally Synchronous (GALS) paradigm in which clocking is done locally at the IP level with global control invoked through asynchronous means. Figure 14.3.1 summarizes the main differences between bus communication systems and NoC structures.

The NoC solution presented is based on a high-throughput 2D-mesh topology with packet switching and wormhole routing. The communication protocol is based on a send/accept scheme at the data link layer; two virtual channels corresponding to different levels of priority guarantee Quality of Service (QoS) at the network layer and a control flow mechanism based on a credit technique avoids deadlock and contention at the transport layer. Each IP core is connected to the NoC by means of a specific Network Interface (NI) for communication and configuration purposes. The communication nodes of the network are implemented using Quasi-Delay-Insensitive (QDI) asynchronous logic that is robust in terms of delay variation due to Process/Temperature/Voltage parameters. This design technique does not require any clock signal but uses a 4-phase handshake protocol and a multi-rail data encoding [2]. An asynchronous/synchronous interface (GALS IF) ensures protocol exchanges between clocked synchronous logic (IP core + NI) and asynchronous logic (node). Figure 14.3.2 presents the components needed to connect an IP core to the network: the NI and the GALS IF are added to the IP core to build the unit that is connected to an asynchronous node. Figure 14.3.3 illustrates the transmission of data from Unit_1 to Unit_2 and the dual-rail encoding that performs the asynchronous handshake protocol. Each unit is clocked individually and the clock frequency of the units is set to reach the best trade-off between timing constraints of the application and power saving policies. In this GALS architecture, there is no global clock signal to be distributed on the whole chip area and no timing constraints between local clocks. Fine grain timing tuning is kept local and so the timing closure problem is solved easily.

This NoC architecture is implemented in the FAUST chip, which is fully functional and is currently used to perform real-time experimentation of advanced MIMO OFDM based telecom techniques foreseen in 4G scenarios [3]. This first experimentation phase will continue with other applications such as 802.11n, 802.16e and 3GPP/LTE. FAUST is structured around a 20-node NoC (see Fig. 14.3.4). Configurable hardwired units ensure high-performance functions for both transmission (TX) and reception (RX) modes. Compute-intensive IPs such as FFT, duo-binary turbo coding, Viterbi and space-time decoding units, are specifically tuned to support data rates up to 100Mb/s per antenna. A fully programmable 6-datapath SIMD structure supports various channel estimation algorithms. Micro-programmed "data moving" engines integrated in RAM units facilitate high-speed data manipulation. An ARM964ES core configures the physical layer units through the network, when necessary. This CPU is also in charge of the lower MAC functions. The on-chip Ethernet interface offers a convenient interface to the upper layers, and a dedicated instrumentation unit measures NoC performance. The chip also includes a reconfigurable data-path (DART module) and a dedicated controller (RAC), which are not used in the telecom context.

A Multi-Carrier OFDM functional diagram (see Fig. 14.3.5) can be mapped on the topological structure of the chip: the data routing between the functional units reflects the sequence of algorithms [4]. Ad hoc micro-programs handle the specific data rearrangements. The process is auto-synchronized: the arrival of data packets triggers the functional processing of the IPs. In this way, the units do not rely on the exact arrival time of data. This makes the system "loosely coupled" and thus easier to modify without changing the global result of the processing. Up to now, application mapping is performed using a manual process but specific tools are under development to automatically map a functional description on the distributed structure.

Figure 14.3.6 presents the main features of the FAUST chip; it is implemented in a 6ML, 130nm, 1.2V, CMOS process from STMicroelectronics. The chip micrograph is shown in Fig. 14.3.7. The whole chip integrates more than 3Mgates and 3.5Mb of embedded RAM, which corresponds to a core area of 72.71mm^2 and a chip area of 79.5mm^2. The maximum NoC throughput measured between 2 adjacent nodes or between an IP and its connected node is 5.120Gb/s per link. The latency is about 6ns per crossed node, 12ns for the GALS IF and 12ns for the NI.

A real-time 100Mb/s SISO OFDM transceiver needs a bandwidth of 10Gb/s that corresponds to a 10% network load, for a complexity of 1.7Mgates at the TX level and 1.9Mgates at the RX level. The integration of each IP within the NoC costs 41Kgates ($\approx$ 0.45mm^2) for the 5×5 asynchronous node (19K), the GALS interface (12K) and the network interface (10K without configuration registers). The 20-node NoC represents about 15% of the overall area and the average complexity of the 23 IP connected is close to 300Kgates (including RAM). Using an optimized frequency scaling scheme, the transceiver functions consume 640mW in TX mode and 760mW in RX mode. The NoC consumption represents only about 6% of the overall consumption for a typical traffic defined by the targeted applications. The cost of the NoC in terms of area is similar to a bus-based architecture, but the properties of NoC structures are better suited to addressing the design issues associated with complex SoCs.

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References:
[1] L. Benini, and G. D. Micheli, "Networks on Chips: A New SoC Paradigm," *IEEE Computer*, vol. 35, pp. 70-78, Jan., 2002.
[2] E. Beigne, et al., "An Asynchronous NoC Architecture Providing Low Latency Service and its Multi-Level Design Framework," *Proc. 11th Inter. Symp. on Advanced Research in Asynchronous Circuits and Systems, ASYNC'2005*, New York, pp. 54-63, March 2005.
[3] R. Rabineau, et al., "Flexible Test-Bed for Real Experimentation of 4G Systems," *15th IST Mobile Summit, Myconos*, p. N°792, pp.1-5, June 4-8, 2006.
[4] N. Chapalain, D. Mottier, and D. Castelain, "Performance of Uplink SS-MC-MA Systems with Frequency Hopping and Channel Estimation Based on Spread Pilots," *PIMRC 2005*, Berlin, pp. 1515-1519, Sept., 2005.

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	Bus	NoC
Structure	**Centralized**	**Distributed**
Scalability	**Low** (the bandwidth is shared by the connected IPs)	**High** (bandwidth increases with the number of IPs)
Implementation	**Complex** (long wires have to be managed)	**Easy** (only local wires exist, floorplanning is modular)
GALS approach	**Complex** (synchonization blocks must be inserted in the centralized structure)	**Easy** (synchronization is made automatically by the asynchronous NoC)
Power consumption	**High** (only a global power saving technique can be used)	**Low** (leakage can be managed locally at communication node level)
Reconfigurability	**Complex** (must be managed inside the IPs)	**Easy** (network interface integrates specific features for application control)

Figure 14.3.1: Bus / NoC comparison.

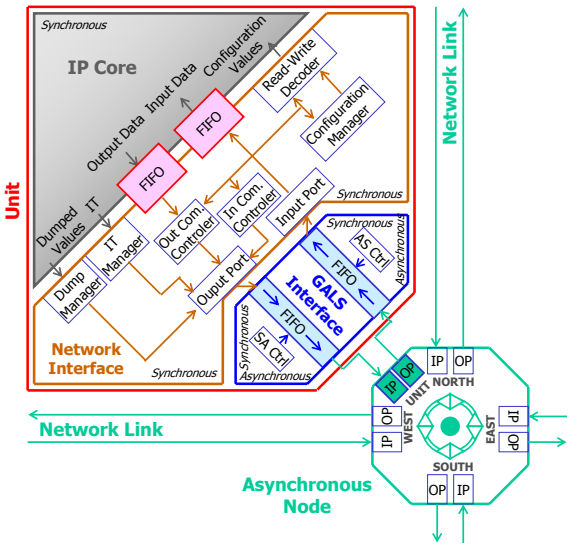


Figure 14.3.2: IP integrated in the NoC.

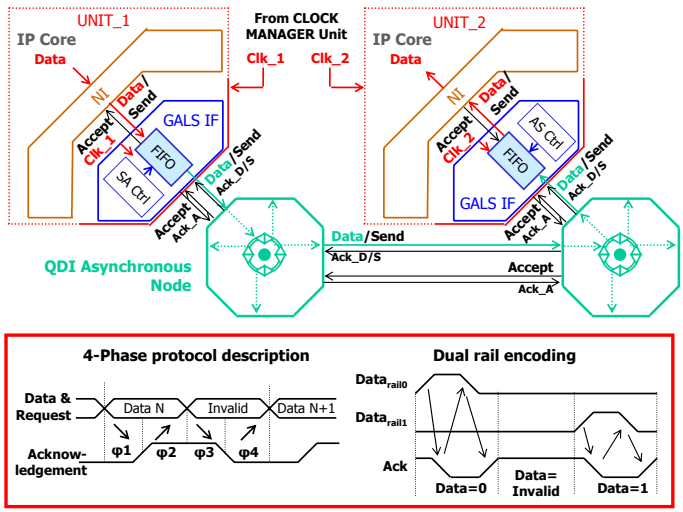


Figure 14.3.3: Asynchronous implementation of the NoC.

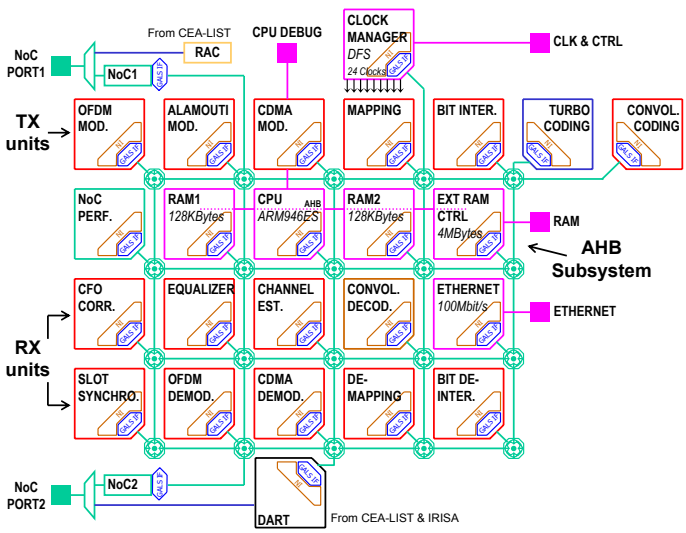


Figure 14.3.4: FAUST block diagram.

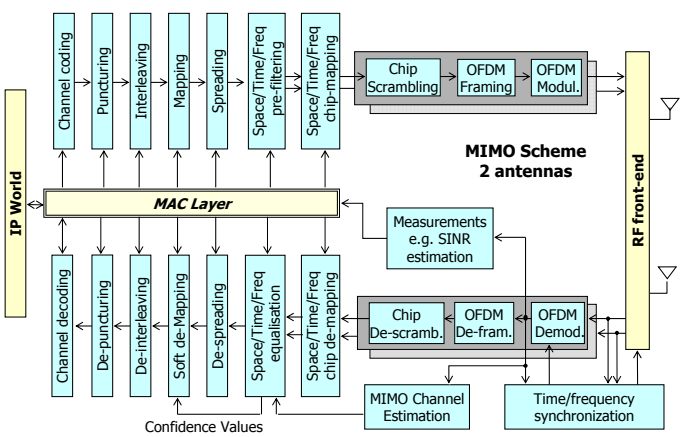


Figure 14.3.5: Telecom functional diagram.

NoC Architecture		
	Topology and Size	2D-Mesh including 20 nodes
	Switching and Routing Modes	Packet switching and Wormhole routing
	Flow Control Technique	Credit Based
	Flit Size (i.e. Word size)	32 bits
	QoS Support	2 Virtual Channels
	I/O	Direct external NoC accesses
	Implementation	Asynchronous Logic (QDI)
	Power Saving Technique	Dynamic Frequency Scaling
Computing and Memory Aspects		
	IP Count	23 Units connected to the NoC
	Processor Core	ARM946ES
	DMA Engines	3 Units to manage on-chip and off-chip memories
	Reconfigurable Datapath	SIMD structure for channel estimation
	Host Computer Interface	100 Mbit/s Full Duplex Ethernet Unit
Technology and Complexity		
	Process	130 nm CMOS 6ML (STMicroelectronics)
	Logic Gate Count	3.124 M Gates (excluding SRAM blocks)
	On-chip Clocks	24 Clocks
	Die Size	8.900 mm * 8.933 mm = 79.50 mm^2
	Package	BGA420 (35 mm * 35 mm)
	Signal I/O Count	275
	Supply Voltage	1.2 V Core, 3.3V I/O
Measured Performances		
	NoC Throughput	5.120 Gbps per link
	IP Operating Frequency	162 MHz
	Chip power Consumption	640 mW TX mode, 760 mW RX mode
	NoC Area	15% of the global area
	NoC Power Consumption	6% of the global consumption

Figure 14.3.6: Chip features.

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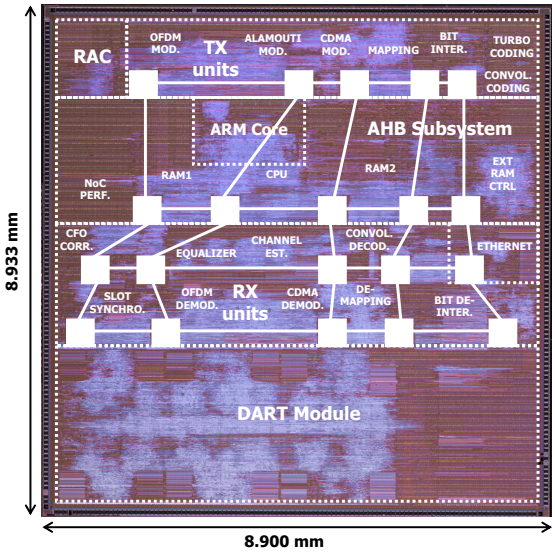


Figure 14.3.7: FAUST chip micrograph.

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